WHAT IS CLAIMED IS:

1. A switching mode power supply comprising:

a rectifier configured to convert AC power to a first DC power;

an output unit configured to convert the first DC power to a second DC power under the control of a first switch; and

a pulse width modulation generator coupled to control the first switch, the pulse width modulation generator having a regulator configured to regulate the first DC power, the regulated first DC power powering the pulse width modulation generator, the regulator comprising a second switch coupled to control a transmitter so that when the second switch is in a first state the transmitter transmits the first DC power to a capacitor to charge the capacitor, and when the switch is in a second state the transmitter does not transmit the first DC power to the capacitor to thereby allow the charge in the capacitor to reduce.

2. The switching mode power supply of claim 1 wherein the regulator further comprises a power supply voltage manager configured to bias the second switch so that during normal mode of operation the regulated first DC power is maintained at a substantially constant voltage level.

3. The switching mode power supply of claim 2 wherein the regulator further comprises a switch core coupled between the power supply voltage manager and the second switch so that during a power up mode the switch core biases the second switch in the first state until the regulated first DC power reaches a predetermined power level, and during the normal mode of operation the switch core couples an output of the power supply voltage manager to the second switch.

4. The switching mode power supply of claim 2 wherein the power supply voltage manager comprises a comparator configured to compare a first voltage derived from the regulated first DC power to a reference voltage and in response output a signal for biasing the second switch such that the regulated first DC power is maintained at the substantially constant voltage.

5. The switching mode power supply of claim 2 wherein the regulator is a switched-mode regulator.

5. An SMPS (switching mode power supply) comprising:

a power supply for converting AC power to DC power and outputting the DC power;

an output unit including a transformer having a primary coil, one end of which is coupled to the power supply, for outputting the power transmitted to a secondary coil of the transformer from the power supply;

a switching driver including a first switch coupled to another end of the primary coil of the transformer, and a first capacitor for generating a second power according to the first power applied by the power supply, for generating PWM (pulse width modulation) signals according to the second power to drive the first switch; and

a feedback circuit for feeding back the power output by the output unit to the switching driver,

wherein the switching driver comprises:

a high-voltage regulator for supplying the first power to the first capacitor when the level of the second power charged in the first capacitor is less than a first level, and intercepting the first power applied to the first capacitor when the level of the second power is greater than a second level;

a PWM generation unit for generating the PWM signals and supplying them to the first switch; and

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the second power reaches a predetermined level, and controlling the operation of the PWM generation unit.

6. The SMPS of claim 5, wherein the high-voltage regulator comprises:

a JFET for lowering the level of the first power; and

a second switch for forming or intercepting a current path between the JFET and the second capacitor in response to an enable signal from the UVLO/bandgap unit.

7. The SMPS of claim5, further comprising:

an oscillator for generating clock signals by control of the UVLO/bandgap unit, and supplying the clock signals to the PWM generation unit; and

a comparator for comparing a feedback voltage supplied by the feedback circuit with the outputs of the oscillator, wherein the PWM generation unit controls the duty ratio of the PWM signals according to comparison results of the comparator.

8. The SMPS of claim 5, wherein the switching driver further comprises a protector for starting operation when the output voltage of the output unit is overloaded, and preventing generation of the PWM signals.

9. The SMPS of claim 8, wherein the switching driver further comprises a controller for outputting an enable signal for a predetermined time when the voltage of the second power is greater than a threshold voltage, and

the protector controls the PWM generation unit to generate the PWM signals for the predetermined time in response to the enable signal from the controller.

10. The SMPS of claim 5, wherein the power supply comprises:

a full-wave bridge rectifier for receiving the AC power and rectifying the same; and

a second capacitor for smoothing the power rectified by the full-wave bridge rectifier.

11. The SMPS of claim 1, wherein the feedback circuit comprises:

an amplifier for amplifying the power output by the output unit;

a photo coupler for starting operation when the power amplified by the amplifier reaches a predetermined level; and

a second capacitor for charging the current supplied by the photo coupler to provide a feedback voltage.

12. An SMPS (switching mode power supply) comprising:

a transformer for receiving DC power at one end of the primary coil, and outputting power through the secondary coil; and

a switching driver including a transistor coupled between another end of the primary coil and a reference voltage, for generating PWM (pulse width modulation) signals for periodically turning on/off the transistor to apply the PWM signals to a gate of the transistor, and operating the transformer by on/off operations of the transistor, wherein

the switching driver comprises:

a capacitor for being charged with a power supply voltage for generating the PWM signals;

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the power supply voltage reaches a predetermined level;

a high-voltage regulator including: a switch for forming a path between the power supply voltage and the capacitor when the power supply voltage charged in the capacitor is less than a first level, and intercepting the path when the power supply voltage is greater than a second level; and a switch core for controlling on/off operations of the switch according to an enable signal supplied by the UVLO/bandgap unit;

an oscillator for generating clock signals according to operation by the UVLO/bandgap unit; and

a PWM generation unit for generating the PWM signals according to the clock signals.

13. The SMPS of claim 12, further comprising a feedback circuit for generating a feedback voltage according to an output of the transformer, and supplying the feedback voltage to the switching driver, wherein

the PWM generation unit controls the duty ratio of the PWM signals according to the feedback voltage.

14. The SMPS of claim 13, further comprising:

a protector for turning off the transistor when the power supply voltage is overloaded or when the feedback voltage is an over-voltage; and

a controller for outputting an enable signal to the protector when the power supply voltage is greater than a threshold voltage during the operation of the protector, wherein

the protector intermittently operates the PWM generation unit according to the enable signal from the controller.

15. A PWM (pulse width modulation) signal generator including a transistor coupled between the primary coil of the transformer and a reference voltage, for supplying PWM signals to a gate of the transistor to periodically turn on/off the transistor and thus operate the transformer, comprising:

a high-voltage regulator including a JFET for receiving DC power and lowering a level of the DC power;

a capacitor for being charged with the current supplied by the high-voltage regulator to form a power supply voltage;

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the power supply voltage charged in the capacitor reaches a predetermined level;

an oscillator for generating clock signals according to control by the UVLO/bandgap unit; and

a PWM generation unit for generating the PWM signals according to the clock signals supplied by the oscillator, wherein

the high-voltage regulator supplies the DC power to the capacitor when the level of the voltage charged in the capacitor is less than a first level, and intercepts the DC power supplied to the capacitor when the level of the voltage charged in the capacitor is greater than a second level.

16. The SMPS of claim 15, wherein the high-voltage regulator further comprises:

a power supply voltage manager for regulating the power supply voltage charged in the capacitor;

a switch core for receiving an enable signal generated by the UVLO/bandgap unit and transmitting a control signal according to a voltage from the power supply voltage manager;

a switch being tuned on/off according to the control signal; and

a current transmitter for coupling the JFET to the capacitor when the switch is turned off, and intercepting the coupling of the JFET to the capacitor when the switch is turned off.

17. The SMPS of claim 15, comprising:

a source/sink unit for receiving the voltage output by the transformer as a feedback voltage to determine a level of the feedback voltage; and

a comparator for comparing an output of the source/sink unit with an output of the oscillator, wherein

the PWM generation unit controls the duty ratio of the PWM signals according to a comparison result of the comparator.

18. The SMPS of claim 17, further comprising:

a protector for turning off the transistor when the power supply voltage is overloaded or when the feedback voltage is an over-voltage; and

a controller for outputting an enable signal to the protector when the power supply voltage is greater than a threshold voltage during the operation of the protector, wherein

the protector intermittently operates the PWM generation unit according to the enable signal from the controller.